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Reg. No. : .....

Name : .....

Fifth Semester B.Tech. Degree Examination, November 2014
(2008 Scheme)
08.503 : COMPUTER ORGANISATION & ARCHITECTURE (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Explain various steps involved in execution of an instruction.
2. Define the performance measures throughput and MIPS.
3. Explain various instruction formats in MIPS.
4. Compare the features of SRAM and DRAM.
5. What are big endian and little endian in association with storage of bytes ? Explain.
6. Give the functions of 8086 pins :

   ALE, RESET and $\overline{TEST}$
7. Explain base indexed addressing mode of 8086 with an example.
8. Explain any three datapath elements.
9. Explain the features of microprogrammed control unit.
10. What is hazard ? Give an example for data hazard situation. Explain.

(10×4=40 Marks)

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – 1

11. a) Explain any 4 addressing modes of MIPS with examples.

    b) Explain the meanings of following instructions in MIPS : j 2000, jal 2000 and jr $ ra.

12. a) Explain any 5 instructions under logical group in MIPS.

    b) Represent the numbers – 12.375_{10} in double precision floating point notation.

13. a) Explain 3rd version of multiplication algorithm with a flowchart.

    b) Use the algorithm above to multiply two binary numbers 1010 and 0011.

Module – 2

14. Draw the datapath for different operations in MIPS with single cycle implementation. Explain various control signals.

15. Draw the state diagram for deriving control signals for R type, lw, sw, conditional branch and jump instructions. Explain how it is implemented with microprogrammed control unit.

16. Write briefly about pipeline hazards.

Module – 3

17. Draw the internal architecture of 8086 and explain about bus interface unit.

18. a) Distinguish between memory mapping and I/O mapping.

    b) Write a note on DMA data transfer mechanism.

19. A memory system contains a cache, main memory and a virtual memory. The access time of cache in 5ns, and has 80% hit rate. The access time of main memory is 100ns with 99.5% hit rate. The access time of virtual memory is 10 ms. What is the average access time ? **(3×20=60 Marks)**